ADVANCED INFORMATION

PE4302

Unique RF Digital Attenuator 6-bit, 31.5 dB, DC – 2.2 GHz

Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Unique power-up state selection
- High attenuation accuracy over temperature and frequency
- Single-supply operation
- Flexible parallel and serial programming interfaces
- Positive CMOS control logic
- 50Ω impedance
- Very low power consumption
- Packaged in a 4x4 MLP

Product Description

The PE4302 is a high linearity, 6-bit RF Digital Step Attenuator "DSA" covering a 31.5 dB attenuation range in 0.5 dB steps. This 50-ohm RF DSA provides both parallel and serial CMOS control interface operates on a single 3-volt supply and maintains high attenuation accuracy over frequency and temperature. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The PE4302 exhibits very low insertion loss and low power consumption. This functionality is delivered in a 4x4mm MLP footprint.

The PE4302 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

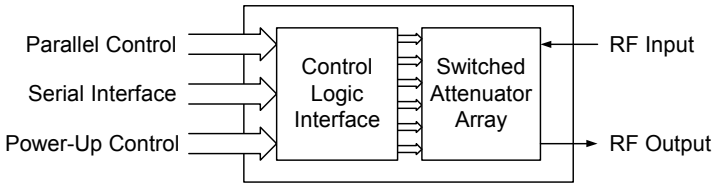


Table 1. Electrical Specifications @ +25 °C

Parameter	Test Conditions	Frequency	Minimum	Typical	Maximum	Units
Operation Frequency			DC		2200	MHz
Insertion Loss		DC to 2.2 GHz	-	2.0		dB
Attenuation Accuracy	Any Bit or Bit Combination	DC to < 1.5 GHz 1.5 to ≤ 2.2 GHz	-	-	±(0.2 + 3% of atten setting) ±(0.2 + 5% of atten setting)	dB dB
1 dB Compression		1 MHz to 2.2 GHz	-	25	-	dBm
Input IP3	Two-tone inputs up to +5 dBm	1 MHz to 2.2 GHz	-	45	-	dBm
Return Loss		DC to 2.2 GHz	15	-	-	dB
Switching Speed	50% control to 0.5 dB of final value		-	-	1	µs
I_{DD} Total Supply Current	V_{DD} = 3V	DC to 2.2 GHz	-	-	300	µA

Figure 2. Pin Configuration (Top View)

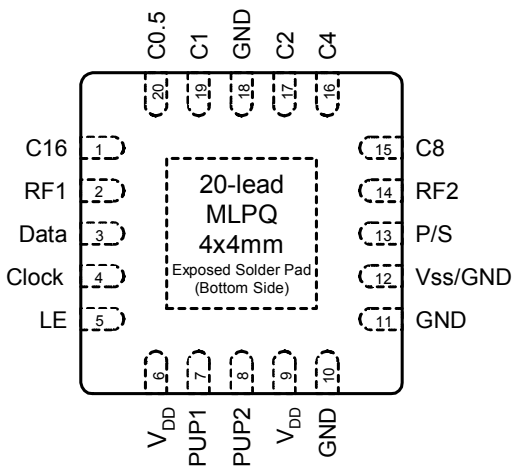


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C16	Attenuation control bit, 16dB.
2	RF1	RF port (Note 1).
3	Data	Serial interface data input.
4	Clock	Serial interface clock input.
5	LE	Latch Enable input (Note 2).
6	V_{DD}	Power supply pin.
7	PUP1	Power-up selection bit, MSB.
8	PUP2	Power-up selection bit, LSB.
9	V_{DD}	Power supply pin.
10	GND	Ground connection.
11	GND	Ground connection.
12	V_{SS}/GND	Negative supply voltage or GND connection(Note 3)
13	P/S	Parallel/Serial mode select.
14	RF2	RF port (Note 1).
15	C8	Attenuation control bit, 8dB.
16	C4	Attenuation control bit, 4dB.
17	C2	Attenuation control bit, 2dB.
18	GND	Ground connection.
19	C1	Attenuation control bit, 1dB.
20	C0.5	Attenuation control bit, 0.5dB.

Note 1: Both RF ports must be DC blocked with an external series capacitor or held at $0V_{DC}$.
2: Latch Enable (LE) has an internal pullup resistor to V_{DD}
3: Connect pin 12 to GND to enable -3V internal supply generator. Connect pin 12 to V_{SS} (-3V) to bypass and disable internal -3V supply generator. See paragraph "Switching Frequency."

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		33	dBm
V_{ESD}	ESD voltage (Human Body Model)		200	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current			300	µA
Digital Input High	0.7xV_{DD}			V
Digital Input Low			0.3xV_{DD}	V

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Switching Frequency

The PE4302 has a maximum 25kHz switching rate when the internal -3V negative supply generator is used (pin 12=GND). The rate at which the PE4302 can be switched is not limited if an external -3V supply is provided. (Pin 12=V_{SS}).

Programming Options

The PE4302 provides very flexible attenuation state programming options that include parallel and serial interfaces, and a unique programming interface for selection of the power-up attenuation state.

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE4302. The "P/S" bit provides this selection, with P/S=LOW selecting the parallel interface and P/S=HIGH selecting the serial interface.

Parallel Interface

The parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in Table 5. These inputs are buffered by a transparent latch that is controlled with the Latch Enable (LE) line. The latch appears transparent to parallel control line data when LE is held HIGH. When LE is taken LOW, data that meets the setup time is latched.

The parallel interface timing requirements are defined by Figure 10 (Parallel Interface Timing Diagram) and Table 9 (AC Characteristics).

Table 5. Truth Table Parallel Interface Mode

P/E	LE	C16	C8	C4	C2	C1	C0.5	Attenuation State
0	1	0	0	0	0	0	0	Reference Loss
0	1	0	0	0	0	0	1	0.5 dB
0	1	0	0	0	0	1	0	1 dB
0	1	0	0	0	1	0	0	2 dB
0	1	0	0	1	0	0	0	4 dB
0	1	0	1	0	0	0	0	8 dB
0	1	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in table.

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 9 (Serial Interface Timing Diagram) and Table 8 (AC Characteristics).

Power-up Control Settings

The PE4302 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S=1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S=0) with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in Table 6 (Power-Up Truth Table, Parallel Mode).

Table 6. Power-Up Truth Table, Parallel Interface Mode

P/S	LE	PUP2	PUP1	Attenuation State
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31 dB
0	1	X	X	Defined by **C0.5-C16**

Note: Power up with LE=1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

Typical Performance Data (V_{DD}=3.0V, 25°C)

Figure 3. Insertion Loss Vs. RF Frequency

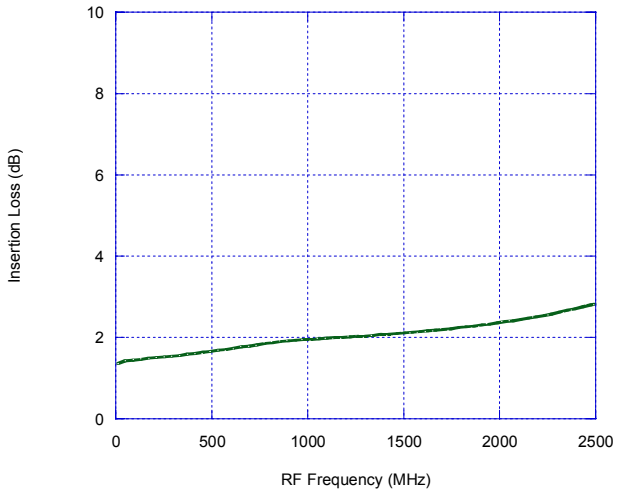


Figure 4. Attenuation at Major steps (Normalized to Insertion Loss)

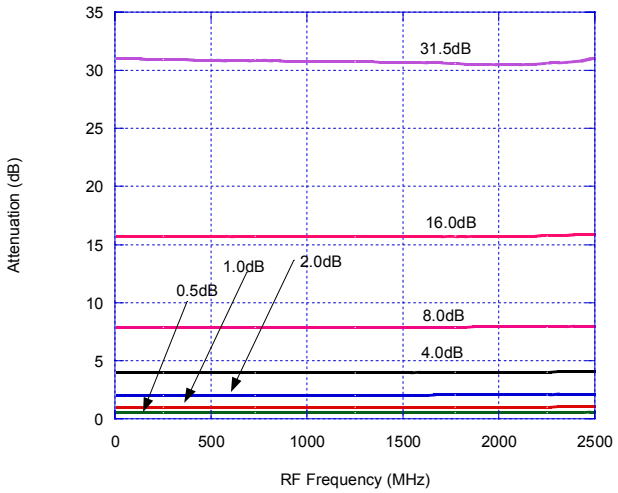


Figure 5. Input Return Loss at Major Attenuation Steps Vs. Rf Frequency

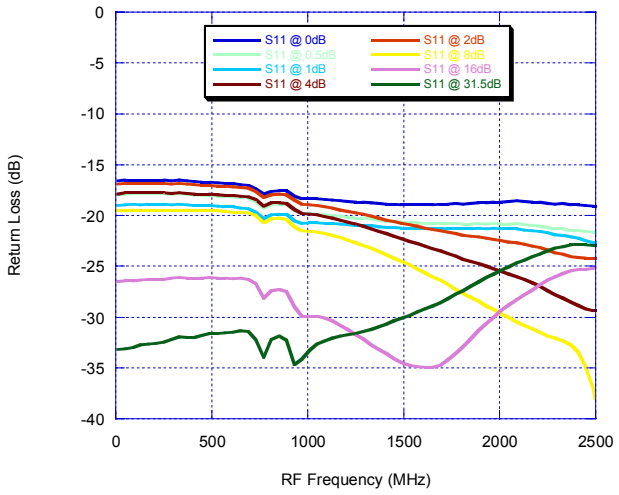


Figure 6. Output Return Loss at Major Attenuation Steps Vs. Rf Frequency

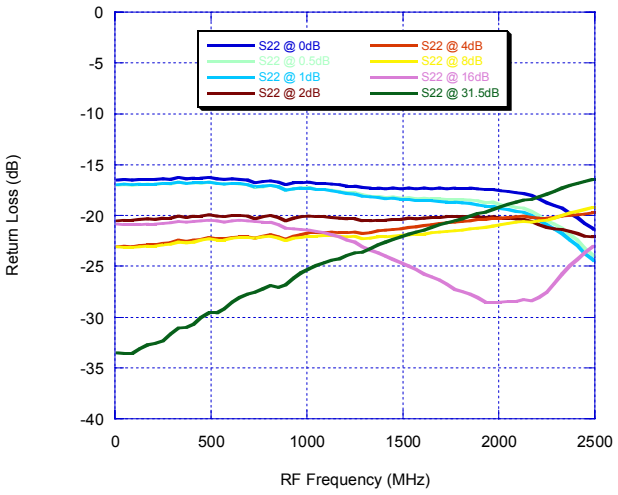
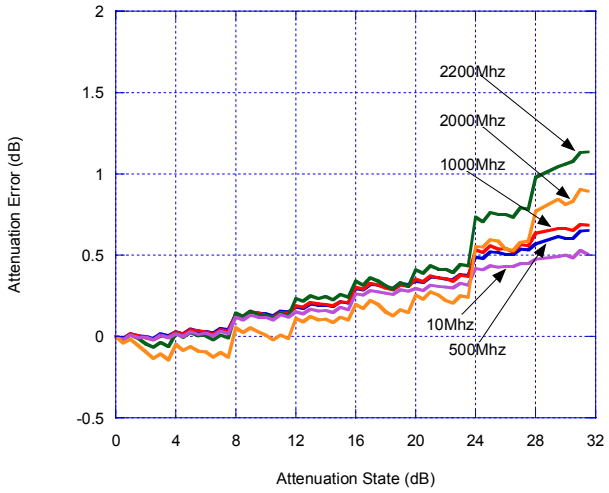


Figure 7. Attenuation Error Vs. Attenuation Setting



Evaluation Kit Information

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE4302 Digital Attenuator.

J9 is used in conjunction with the supplied DC cable to supply VDD, GND, and –VDD. If use of the internal negative voltage generator is desired, then connect –VDD (Black banana plug) to GND. If an external –VDD is desired, then apply -3V.

J1 should be connected to the parallel port of a PC with the supplied ribbon cable. The evaluation software is written to operate the DSA in serial mode, so Switch 7 (P/S) should be ON with all other switches off. Using the software, enable or disable each attenuation setting to the desired combined attenuation. The software automatically programs the DSA each time a attenuation state is enabled or disabled.

To evaluate the Power up options, first disconnect the parallel ribbon cable from the evaluation board. The parallel cable must be removed to prevent the PC parallel port from biasing the control pins to unknown states. During power up in serial mode (P/S=1), the default power-up signal attenuation is set to the value present on the six control bits on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

To power up in Parallel mode (P/S=0) with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in the Truth table below.

P/S	LE	PUP2	PUP1	Attenuation State
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31 dB

Figure 8. Evaluation Board Layout

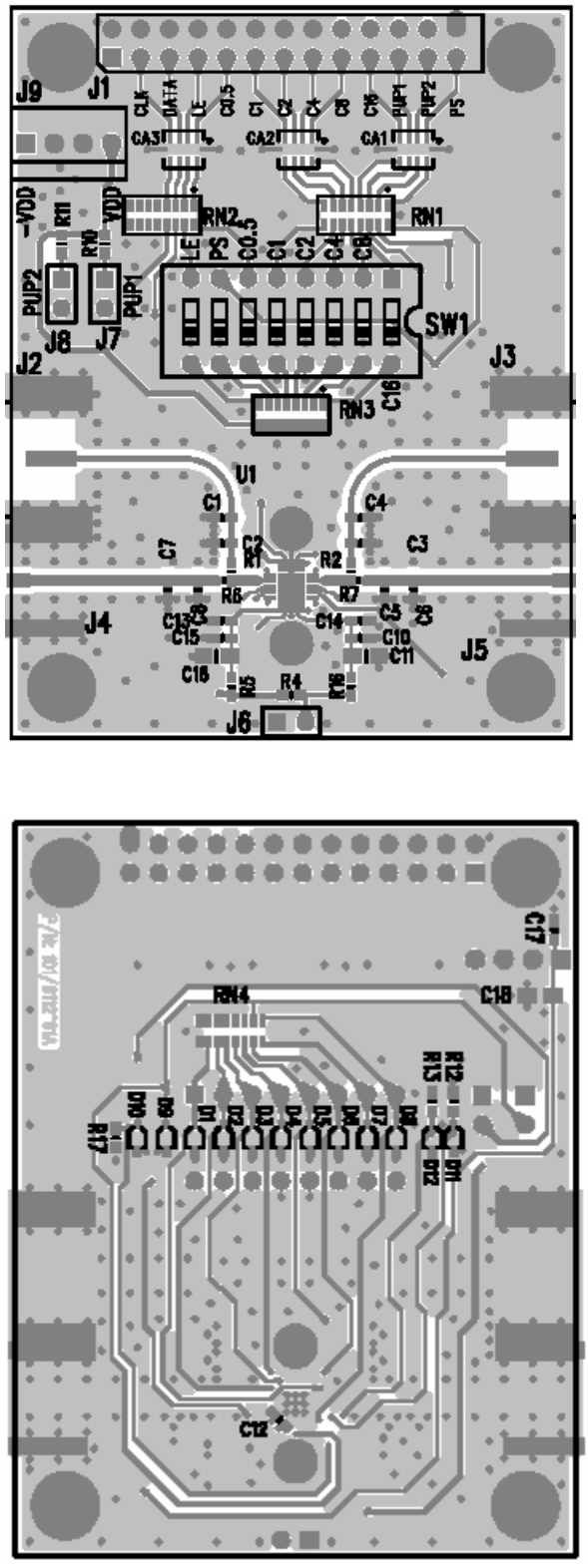


Figure 9. Serial Interface Timing Diagram

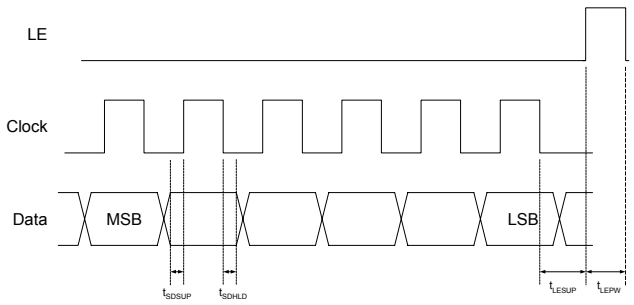


Table 7. 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) LSB (last in)

Figure 10. Parallel Interface Timing Diagram

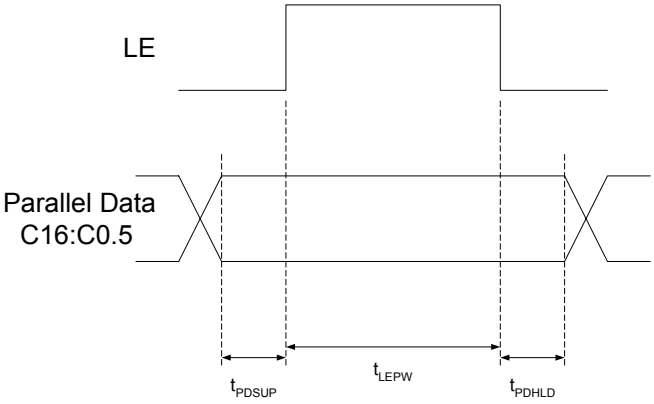


Table 8. Serial Interface AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency (Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

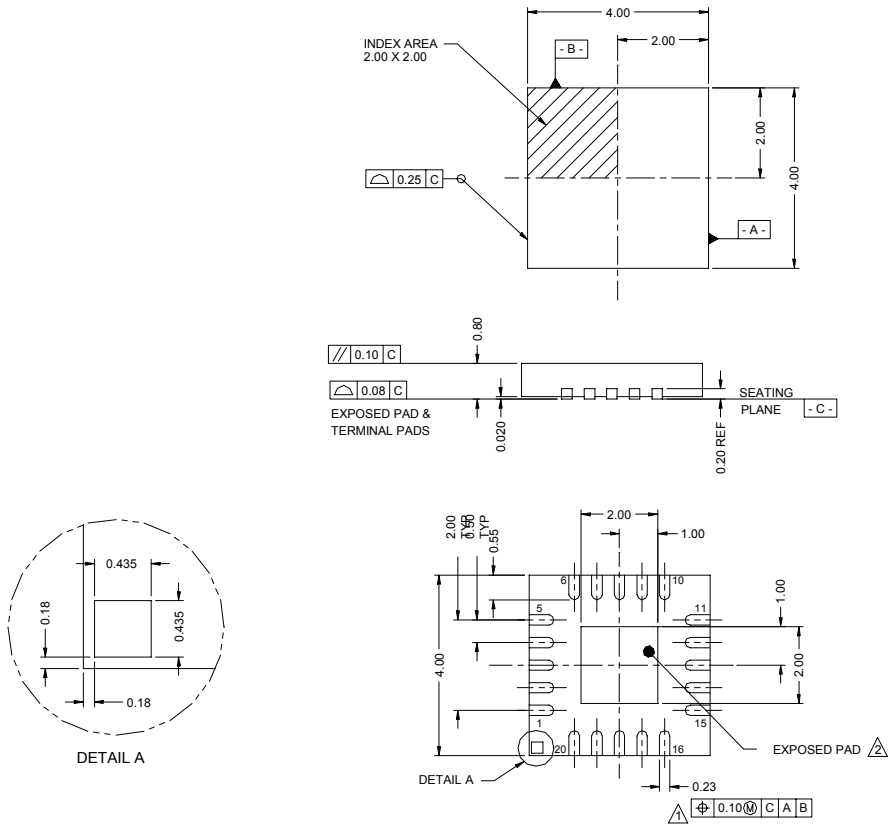
Note 1: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Table 9. Parallel Interface AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before rising edge of LE	10		ns
t_{PDHLD}	Data hold time after falling edge of LE	10		ns

Figure 11. Package Drawing



1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.
2. CCOPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. DIMENSIONS ARE IN MM.

Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4302-01	4302	PE4302-20MLP4x4-92A	20-lead MLPQ	91 units / Tube
4302-02	4302	PE4302-20MLP4x4-6000C	20-lead MLPQ	3000 units / T&R
4302-00	PE4302-EK	PE4302-20MLP4x4-EK	Evaluation Board	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).